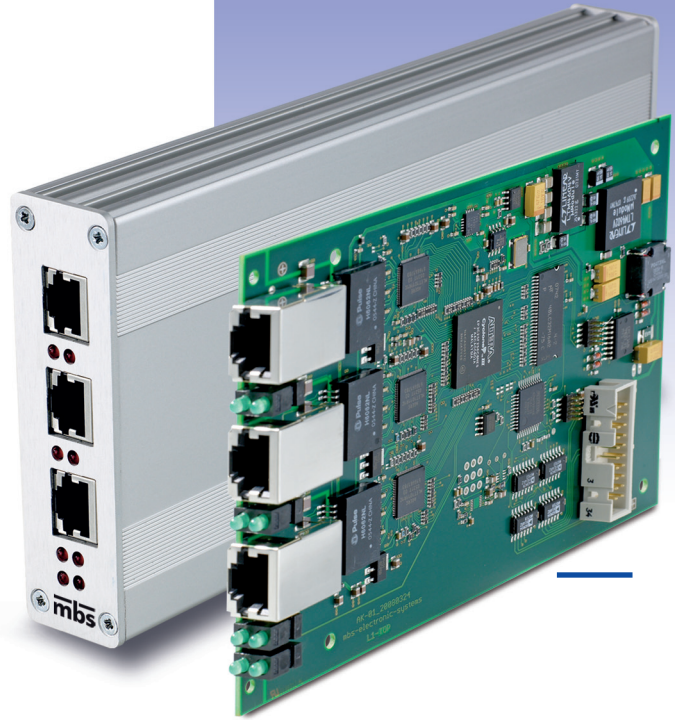


## AFDX® / ARINC 664 Gateway to Gigabit Ethernet

with High Performance Bus  
Monitoring and Test Features



### Features

- AFDX® / ARINC 664 Full Duplex operation at 10 / 100 / 1000 Mb/s
- Gigabit Ethernet Network with UDP/IP
- 256 VL / Sub-VL Transmit Ports
- 256 VL Receive Ports
- Traffic Scheduling via VL and BAG Configuration
- Receive Filtering of combined VL, Network, UDP Addresses
- Full AFDX® / ARINC 664 Bus Monitoring
- Fault Insertion and Detection
- 16 MB Message Buffering
- IRIG-B time code decoder
- Time Stamping with 16ns Resolution

The ÆSyBus 664 Module provides a unique high performance means to interface ARINC-664 data bus with almost any serious computer and operating system using standard Gigabit Ethernet and UDP/IP protocol. It avoids the possible processing bottlenecks, common to many AFDX® / ARINC-664 interface solutions by automatically distributing incoming messages on to a network of distributed computers communicating in full duplex mode at 1000 M bits /s. (Ten times the speed of AFDX® / ARINC-664).

The concept is very simple. The ÆSyBus 664 Module sits between an AFDX® / ARINC-664 network and a standard Gigabit Ethernet network providing the function of a Gateway which captures assigned messages on one network and automatically translates them into messages on the other network, while rigorously following appropriate protocol requirements. The consequence is that many networked computers have a simple and direct access to AFDX® / ARINC-664 network, to send and receive messages, monitor network events, insert and detect faults. In fact all the requirements necessary to thoroughly Test and Monitor AFDX® / ARINC-664 network activity and communicate with aircraft equipment.

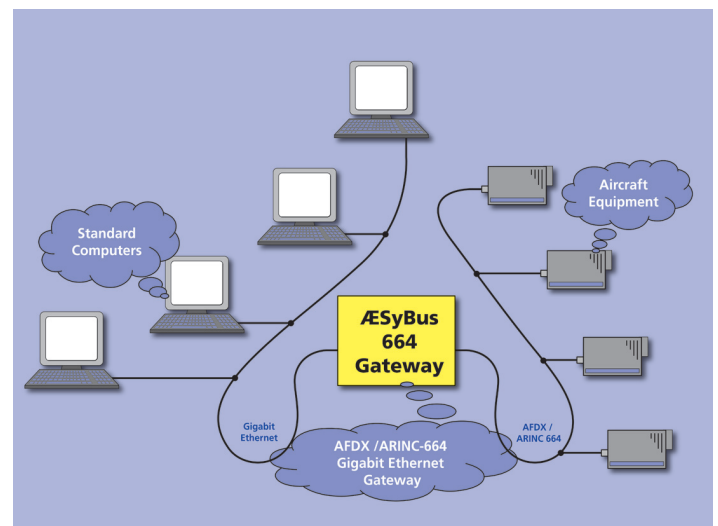


Figure 1: ARINC-664 / Gigabit Ethernet Gateway Operational Concept

### Description

The Gateway is accessed over the Gigabit Ethernet Network using UDP/IP protocol. UDP port addresses are grouped according to the three major functions: Configuration, Control and Status Monitoring; ARINC-664 Virtual Link (VL) Transmission; and, ARINC-664 VL Reception. See Figure 2.

Up to 10 separate Users can log on to the Gateway: Configure the AFDX® / ARINC-664 VL Transmit and Receive Ports and configure the Host Messaging system to send regular AFDX® / ARINC-664 Status messages over the Network.

256 UDP Ports provide access to the Transmit VL FIFO buffers. Each VL FIFO can buffer up to 16 AFDX® / ARINC-664 message packets. Each FIFO is assigned a VL and each VL assigned a BAG value for scheduling VL messages on the AFDX® / ARINC-664 network. Several VL FIFO buffers can be assigned to the same VL to provide

sub-VL buffering. The VL Scheduler has the capacity to schedule 256 unique VL channels.

The user sends the AFDX® / ARINC-664 data in standard UDP/IP message packets to the Transmit VL Ports. The Gateway buffers the VL streams, replaces the MAC, IP and UDP addresses by the assigned VL addresses, makes other protocol adjustments and then schedules the messages on to the Dual Redundant AFDX® / ARINC-664 network in accordance with the assigned BAG values. By using standard UDP/IP protocol, the Gateway can be accessed via any computer and operating system which has an Ethernet Interface and supports internet protocol. There is no requirement for special protocol or driver software.

Reception operates in a similar way to Transmission. Data is captured on both redundant AFDX® / ARINC-664 buses and any duplicated frames dropped. The protocol headers are checked for validity and type, and, if appropriate, the frames are filtered prior to dispatching to the configured host addresses. Message filtering is made on the combined VL ID, Network ID and UDP Port. The destination MAC, IP and Port addresses for identified messages are replaced by addresses assigned to the receive VL and then dispatched to the appropriate host computers / applications.

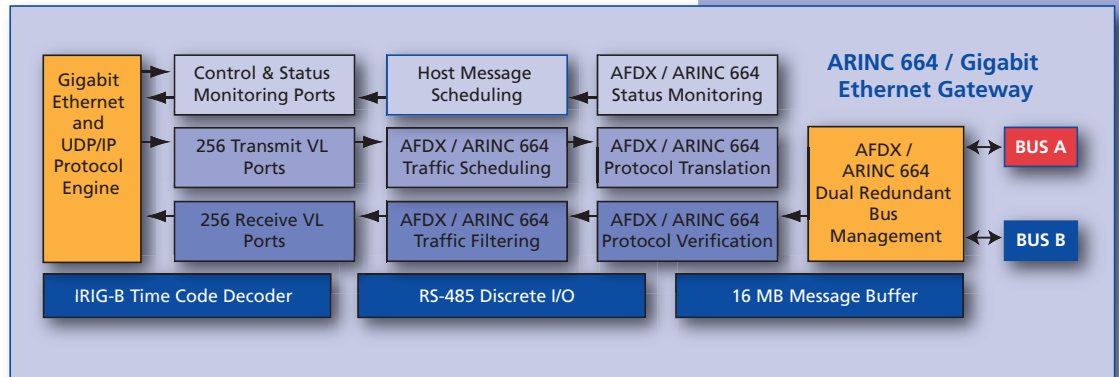


Figure 2: AFDX® / ARINC 664 Gateway to Gigabit Ethernet Functional Block Diagram

All AFDX® / ARINC-664 message packets captured by the Gateway are automatically time-stamped on the rising edge of the receive data valid signal by a 64 bit Timer and with a resolution of 16ns. This time-stamp together with the protocol headers and status information are stored in a cyclic status buffer, prior to dispatch to host applications.

In addition to fault detection, the Gateway can be configured to deliberately insert faults into messages. This is achieved by configuring particular Transmit VL Ports for fault insertion. Messages sent to such ports will automatically create the desired errors.

Support for synchronising time-stamping with other test equipment is provided with an IRIG Time Code Decoder and two pairs of RS-485 Transceivers.

## Specification

### Multiple Host Interface:

- 100 Base-TX, 1000 Base-T Gigabit Ethernet
- Supported Protocols: IP, UDP, ARP, ICMP
- 10 Configuration, Control and Status Monitoring Ports
- 256 AFDX® / ARINC-664 Transmit VL Ports
- 256 AFDX® / ARINC-664 Receive VL Ports

### Test and Monitoring Support:

- 64 bit Time-Stamping with 16ns resolution
- Automatic Monitoring of all AFDX® / ARINC-664 Packet Headers (MAC, Type, IP, UDP)
- Error Insertion and Detection
- IRIG Time Code decoder
- RS-485 Discrete I/O

### Dual AFDX® / ARINC 664 Interfaces:

- 10 Base-T, 100 Base-TX, 1000 Base-T Gigabit Ethernet
- Dual Redundant Bus Management
- AFDX® / ARINC-664 VL Traffic Scheduling (Max. 256 VL)
- AFDX® / ARINC-664 VL Traffic Filtering (Max. 256 VL)
- Filtering per VL, Network, Port
- 256 VL / Sub-VL FIFO Message Buffers (Max. 16 packets / FIFO)

## ÆSyBus 1553 Ordering Information

Part Number	Description
AE-664-VL256FID	Gigabit Ethernet to ARINC 664 Gateway with Bus Monitoring and Test Features and support for 256 ARINC-664 Receive and Transmit Virtual Links

**mbs Electronic Systems GmbH**  
Ringstrasse 3, D-82319 Starnberg  
Tel.: +49 (0) 8151/918047  
Fax: +49 (0) 8151/449646  
info@mbs-electronics.com  
www.mbs-electronics.com

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