

PTP-EX High-Rate Front-End Processor™

APPLICATIONS

- ▶ High-rate remote sensing ground stations
- ▶ Satellite/Payload integration and test
- ▶ Transport of wideband isochronous data over a WAN
- ▶ High-rate bit error rate test system
- ▶ High-rate digital record/playback system
- ▶ Satellite link emulation, testing, and monitoring

KEY FEATURES

- ▶ 1.2 Gbps serial throughput for CCSDS and TDM frame processing and archiving
- ▶ 400 Mbps disk logging of Reed-Solomon corrected CCSDS frames and simultaneous processing of real-time data
- ▶ CCSDS and TDM data simulation with 1.2 Gbps serial output
- ▶ 400 Mbps real-time network transfer
- ▶ Intuitive graphical user interface



The industry's fastest front-end processor. Process, distribute and archive satellite-downlinked CCSDS/TDM frame data at up to 1.2 Gbps.

PTP-EX HIGH-RATE FRONT-END PROCESSOR OVERVIEW The PTP-EX is a high-rate satellite data processing and simulation system that supports both CCSDS (for Conventional and Advanced Orbiting Systems) and Time-Division Multiplexed (TDM) formats, performing data ingest, processing, distribution and archiving functions at rates up to **1.2 Gbps**. It is most commonly deployed within a satellite ground station, but is also ideal for satellite integration and test applications.

HIGH-RATE INGEST, PROCESSING, FORWARDING & ARCHIVING The PTP-EX accepts single or dual downlink data streams, performing frame synchronization, derandomization, Reed-Solomon error correction, CRC decoding, time tagging and logging at rates up to 1.2 Gbps. It also integrates real-time CCSDS packet processing and logging capabilities at data rates beyond 400 Mbps. The system performs CCSDS packet processing, using Virtual Channel Identifier or Application Process Identifier to route data to networked processing centers and concurrently log to disk. Data files can be stored locally, or forwarded to processing centers post-pass.

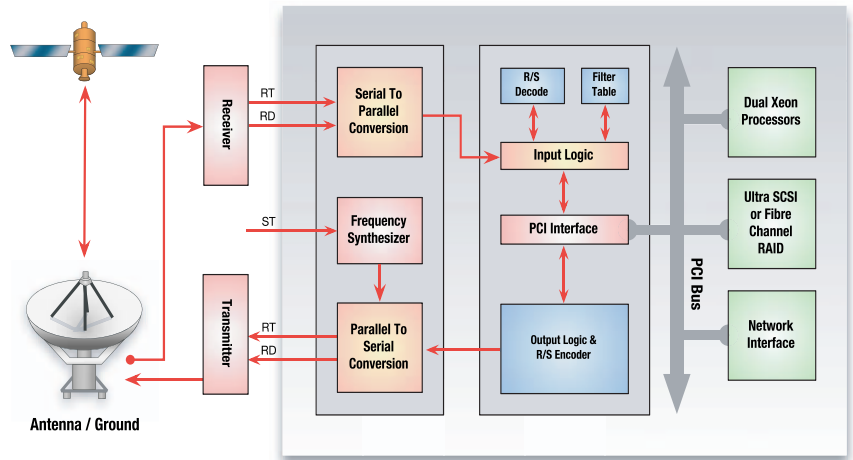
PTP-EX High-Rate Front-End Processor™

ENCRYPTED DOWNLINK SUPPORT The PTP-EX can be used to transport wideband isochronous data over IP or ATM networks for missions with bulk encrypted downlink. In addition to standard CCSDS service processing, it optionally supports AES decryption and Rice decompression.

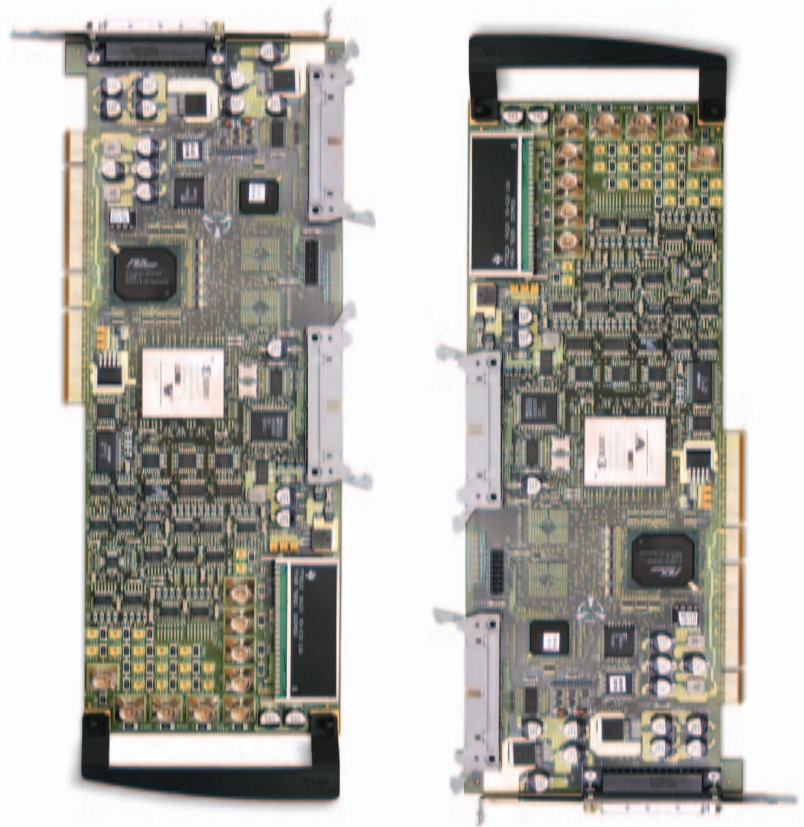
SIMULATION & TEST CAPABILITIES The PTP-EX includes configurable simulation and file playback capability for loopback testing. It also includes a Bit Error Rate Test module for downlink and network path integrity verification.

MISSION-GRADE HARDWARE The PTP-EX is based on a high-performance, high-reliability PCI server architecture with dual Xeon processors, mirrored system drives, hot-swap fans, and redundant power supplies. It provides a 10/100 Ethernet interface for monitor and control, and a Gigabit Ethernet interface for high-speed network data transfer. Storage options include direct attached RAID, FibreChannel Storage Area Network, or Network Attached Storage (NAS).

EASY LOCAL OR REMOTE CONFIGURATION The PTP can be controlled locally or remotely via an intuitive, straightforward graphical user interface. A remote control library is also provided for integration with satellite control systems such as OS/COMET and EPOCH 2000, and a Simple Network Management Protocol (SNMP) agent is available to facilitate integration with management platforms such as HP OpenView.



System architecture of the PTP-EX High-Rate Front-End Processor



The PTP-EX Serial I/O Processing Core The PCI-6550, an innovative PCI-based dual-channel Frame Synchronizer / Data Simulator with QPSK ambiguity resolution, performs high-rate data processing functions within the PTP-EX.

PTP-EX High-Rate Front-End Processor™ Specifications

PTP-EX SPECIFICATIONS

Physical Specifications

- 6U rack-mount chassis
- Dual Xeon 3 Ghz, 2 GB RAM
- Mirrored, hot-swap 2x80Gb SATA HD
- 10/100 Ethernet for monitor & control
- Gigabit Ethernet
- DVD+-RW for program load & data storage

Front-End Processing

- Data rates up to 1.2 Gbps
- Frame synchronization, derandomization, Reed-Solomon decoding, and CRC decoding
- Time tagging and data quality annotation
- CCSDS virtual channel sorting and packet processing
- Advanced Encryption Standard (AES) decryption
- Rice decompression
- Real-time disk logging and high-speed network transfer

Simulation & Testing

- CCSDS and TDM data simulation at rates up to 1.2 Gbps
- CRC encoding, Reed-Solomon encoding, randomization, and convolutional coding
- Data quality monitoring (CCSDS and TDM) and bit/packet error rate testing
- Data logging and playback

Communication Links

- High-performance Gigabit Ethernet and ATM for data transfer, control and monitoring
- Real-time network data transfer (UDP, IP multicast, TCP client/server)
- Support for user encapsulation formats including NASCOM RTP, IPDU, SFDU, LEO-T, EDOS
- Network protocol conversion

Serial I/O

- Data rate from 100 bps to 1.2 Gbps
- Differential ECL with 50-Ohm termination to -2V utilizing SMA female connectors
- Differential ECL with 120-ohm termination utilizing Triax connectors (max data rate 200 Mbps)

Parallel I/O

- Data rates up to 80 MBps
- Configurable as 8-, 16-, or 32-bit input
- Differential TTL interface

Frame Synchronizer

- Frame sync pattern up to 32 bits
- Frame sync mask up to 32 bits
- Sync bit error threshold up to 15 bit errors
- Adaptive sync strategy with 0 to 7 check frames and 0 to 7 flywheel frames]
- Bit slip window from 0 to +/-3 bits
- BPSK or QPSK automatic ambiguity resolution and correction
- Frame length up to 4096 bytes/frame
- Time tagging: 5 usec accuracy with IRIG, 10 MHz & 1 PPS input (IRIG input only, 100 usec)
- Time stamp using internal or external 10 MHz reference and 1 PPS

Reed-Solomon Error Correction Encoding / Decoding

- CCSDS Reed-Solomon (RS) (255,223) error correction
- Support for interleave depth up to 16
- CCSDS Reed-Solomon (10,6) header error correction
- Shortened codeword support using "virtual fill"
- Real-time quality generation and annotation for each VCDU

CRC Error Detection Decoder / Encoder

- Compute frame error control field from received data using the polynomial $g(x) = x^{16} + x^{12} + x^5 + 1$
- Programmable offset from 0 to 8 bytes

Derandomizer / Pseudo-randomizer

- Exclusive OR received from data following sync pattern with pattern given by $h(x) = x^8 + x^7 + x^5 + x^3 + 1$
- Programmable start offset frame 0 to 8 bytes

Data Simulator

- Onboard memory for high-speed simulation
- Hardware sync marker, ID counter, and time stamp insertion
- Programmable clock and data polarity
- Frame length up to 4096 bytes/frame
- Programmable output frequency from 100 Hz to 400 MHz

Convolutional Encoder

- CCSDS rate=1/2, constraint length K=7
- Programmable G1, G2 order
- Programmable inversion of G1 and G2

Test Signal Outputs

- SYNC: sync detect
- CRC_ERR: CRC error detection
- RS_ERR: RS error detection
- VCID_ERR: Invalid VCID detection
- LOS: Lock to Search transition detection
- SOF: Start of output frame detection

PCI Interface

- 64-bit, 66 MHz
- Sustained PCI Bus master transfer to/from I/O buffers at full PCI bandwidth

©2005 Avtec Systems, Inc. All rights reserved. Avtec Systems, the Avtec Systems logo, and the PTP - EX are trademarks of Avtec Systems, Inc. in the U.S. and various countries. All other trademarks are the property of their respective owners. Specifications subject to change without notice.

LEARNING MORE To learn more about Avtec Systems, visit us on the Web at <http://www.avtec.com>.

Corporate Headquarters

14432 Albemarle Point Place
Chantilly, VA 20151 USA
p: [+1] 703-488-2500
f: [+1] 703-488-2555

Avtec Denver & Antenna Group

3033 South Parker Rd, Suite 1210
Aurora, CO 80014 USA
p: [+1] 303-369-4300
f: [+1] 303-369-5175

(MM05-019, rev. 01-05)